REMARKS

The present Amendment amends claims 1-11, 13 and 14 and leaves claim 12 unchanged. Therefore, the present application has pending claims 1-14.

Applicants' Attorney, the undersigned, respectfully requests the Examiner to contact Applicants' Attorney by telephone prior to examination to discuss the outstanding issues of the present application.

Claims 1-14 stand rejected under 35 USC §102(e) as being anticipated by Sanada (U.S. Patent No. 6,484,245). This rejection is traversed for the following reasons. Applicants submit that the features of the present invention as now more clearly recited in claims 1-14 are not taught or suggested by Sanada whether taken individually or in combination with any of the other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Amendments were made to the claims to more clearly describe features of the present invention as recited in the claims. Particularly, amendments were made to the claims to more clearly recite that the present invention is directed to a storage system and a control method implemented in a storage system, wherein the channel controller of the storage system has a particular internal configuration and performs particular processes using tis internal configuration.

According to the present invention the storage system includes a storage controller for controlling the storage system and at least one disk device for storing data from the storage controller.

Further, according to the present invention the storage controller includes a channel controller for receiving a file access input/output (I/O) request based on file-name indication from an information processing device through a network, transmitting/receiving data to/from the information processing device and outputting a block access I/O request corresponding to the file access I/O request, a disk controller for carrying out input/output control of data stored in a storage volume for storing the data based on the block access I/O request output by the channel controller, a first memory including a cache memory for temporarily storing the data delivered between the channel controller and the disk controller, and a data transfer network connected to the channel controller, the disk controller and the first memory.

Still further, according to the present invention the channel controller is equipped with a first processor for outputting the block access I/O request corresponding to the file access I/O request and controlling the first memory, a file access circuit which has a second processor and a second memory controlled by the second processor and serves to control the transmission/reception of the file access I/O request and the data sent from/to the information processing device, a data transfer device for controlling data transfer between the first memory and the second memory, and a third memory controlled by the first processor. The elements of the channel controller are formed on a circuit module.

Still further yet, according to the present invention the second processor transmits information indicating the storage position of the data in the second memory to the first processor, the first processor writes into the third memory data transfer information containing information indicating the

storage position of the data in the first memory and information indicating the storage position of the data in the second memory, and the data transfer device reads out the data transfer information from the third memory and controls the data transfer between the first memory and the second memory based on the data transfer information thus read out.

The above described features of the present invention now more clearly recited in the claims are not taught or suggested by any of the references of record whether taken individually or in combination with each other. Particularly, the above described features of the present invention now more clearly recited in the claims are not taught or suggested by Sanada whether taken individually or in combination with any of the other references of record.

Sanada, relied upon by the Examiner to reject the claims teaches, discloses for example, in Fig. 1 thereof a storage system having a storage controller 40 and at least one disk device 50, wherein the storage controller includes a fibre channel control unit 41, a device (disk) interface control unit 46, a microprocessor 42, control memory 43 and cache control unit and cache memory 44 and 45.

It would appear from the teachings of Sanada that the fibre channel control unit 41 as taught by Sanada corresponds to the channel controller as recited in the claims and the disk interface control unit 46 corresponds to the disk controller as recited in the claims. The cache memory 45 could, for example, correspond to the first memory and it would appear that the controller 40 corresponds to the storage controller recited in the claims since the storage controller 40 as taught by Sanada includes each of the above

described elements namely the fibre channel control unit 41, the disk interface control unit 46, the cache memory 45, etc.

However, at no point is there any teaching or suggestion in Sanada of the internal structure of the fibre channel control unit 41 which corresponds to the channel controller as recited in the claims. In fact, Sanada simply teaches that the fibre channel control unit 41 "maybe a protocol processor including a direct memory access (DMA) for controlling data transmission between it and the host computers 10, 20, 30". The Examiner's attention is directed to col. 4, lines 61-64 of Sanada.

Each of the claims of the present application specifically recite that the channel controller is equipped with a first processor, a file access circuit which has a second processor and a second memory controlled by the second processor, a data transfer device for controlling data transferred between the first memory and the second memory and a third memory controlled by the first processor and that each of these elements perform specific functions individually and in cooperation with others of the elements. There is absolutely no teaching or suggestion in Sanada that the fibre channel control unit 41 includes any of the above described elements nor perform any of the above described functions now recited in the claims.

Further, there is absolutely no teaching or suggestion in Sanada that the fibre channel control unit 41 includes a file access circuit which has a second processor which transmits information indicating the storage position of data in the second memory to the first processor, wherein the first processor writes into the third memory data transfer information containing information indicating the storage position of the data in the first memory and

information indicating the storage position of the data in the second memory as in the present invention. As noted above, Sanada simply teaches that the fibre channel control unit 41 includes a protocol processor including DMA. There is absolutely no teaching or suggestion of first and second processors nor the functions performed by the first and second processors as recited in the claims.

Still further, there is no teaching or suggestion in Sanada that the data transfer device performs various functions including reading out the data transfer information from the third memory and controlling the data transfer between the first memory and the second memory based on the data transfer information read out as in the present invention as recited in the claims. There is absolutely no teaching or suggestion in Sanada of various elements having the specific functions and inter-operational functions thereof as in the present invention as recited in the claims.

Thus, Sanada fails to teach or suggest that the channel controller which forms a part of the storage controller of the storage system is equipped with a first processor for outputting the block access I/O request corresponding to the file access I/O request and controlling the first memory, a file access circuit which has a second processor and a second memory controlled by the second processor and serve to control the transmission/reception of the file access I/O request and the data sent from/to the information processing device, a data transfer device for controlling data transfer between the first memory and the second memory, and a third memory controlled by the first processors, which are formed on a circuit module as recited in the claims.

Further, Sanada fails to teach or suggest the second processor transmits information indicating the storage position of the data in the second memory to the first processor, the first processor writes into the third memory data transfer information containing information indicating the storage position of the data in the first memory and information indicating the storage position of the data in the second memory, and the data transfer device reads out the data transfer information from the third memory and controls the data transfer between the first memory and the second memory based on the data transfer information thus read out as recited in the claims.

Therefore, Sanada fails to teach or suggest the features of the present invention as now more clearly recited in the claims. Accordingly, reconsideration and withdrawal of the 35 USC §102(e) rejection of claims 1-14 as being anticipated by Sanada is respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the reference utilized in the rejection of claims 1-14.

In view of the foregoing amendments and remarks, applicants submit that claims 1-14 are in condition for allowance. Accordingly, early allowance of claims 1-14 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C., Deposit Account No. 50-1417 (TMI-128).

Respectfully submitted,

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.

Carl I. Brundidge
Registration No. 29,621

CIB/jdc
(703) 684-1120